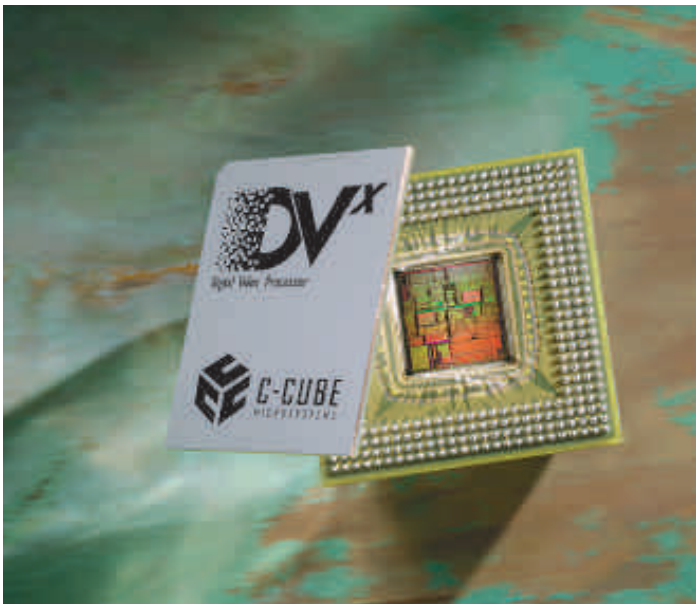
DV^X ARCHITECTURE

A Breakthrough Multimedia Architecture that Integrates MPEG-2 Encoding and Decoding on One Chip

DV^x™ from C-Cube Microsystems is the industry's first MPEG-2 video encoder/decoder (codec) architecture implemented on a single chip. Standing for Digital Video in multiple (or x) platforms, DV^x enables MPEG as a common digital video format across consumer, professional, and prosumer video applications while conserving memory, power, and circuit board space.



DV^X Digital Video Processor

Using C-Cube's leading-edge PerfectView™ encoding algorithm, DV^x digital video processors deliver the highest quality 4:2:0 and 4:2:2 MPEG-2 images available today at significant bit rate savings. What's more, the single-chip implementation enables product designs that reduce cost, increase reliability, and speed time to market.

The scalable DV^x architecture is ideal for high-resolution broadcast applications such as 4:2:2 studio-to-studio video distribution and high-definition television (HDTV). The architecture also offers a compact, economical solution for authoring and nonlinear editing applications, incorporating features such as multiple-stream decoding and a rich portfolio of video post-processing capabilities.

C-Cube is the leading developer of integrated circuits, modules, and software for video compression and decompression. DV^x is the most advanced stage in a technology evolution that began with the 1993 introduction of the world's first MPEG video encoder, the Emmy Award winning C-Cube VideoRISC Compression Processor (VRP).

DV^X Platform

DV^x incorporates an advanced platform architecture designed to efficiently implement fully compliant MPEG-2 compression in real time. Depending on the target application, DV^x products can consist of one or more chips, plus application software in the form of downloadable microcode.

C-CUBE MICROSYSTEMS

The 32-bit embedded RISC CPU instruction set has been extended for efficient MPEG compression, decompression, and special video effects. A programmable Motion Estimation Coprocessor (ME) takes commands from the CPU and performs hierarchical motion estimation on designated frames.

The digital signal processing (DSP) coprocessor performs approximately 1.6 billion arithmetic, pixel level operations per second.

The DV^x Interprocessor Communications (IPC) capability provides the interface between multiple DV^x chips to support higher quality and resolution.

The video interface is a programmable high-speed I/O port allowing the transfer of uncompressed digital video into and out of the DV^x processor. The serial audio interface can capture up to eight channels of uncompressed 16- and 24-bit digital audio from an external audio codec. The synchronous dynamic random access memory (SDRAM) controller interface generates the addressing and controlling signals necessary to support the local SDRAM. All applications use four 16 Mbit SDRAMs totaling 8 MB of external storage running at a clock speed of 100 MHz.

PCI Bus mastering allows easy integration with PCs and workstations using a PCI host bus compliant with PCI Local Bus Specifications Revision 2.1.

Key DV^x Features

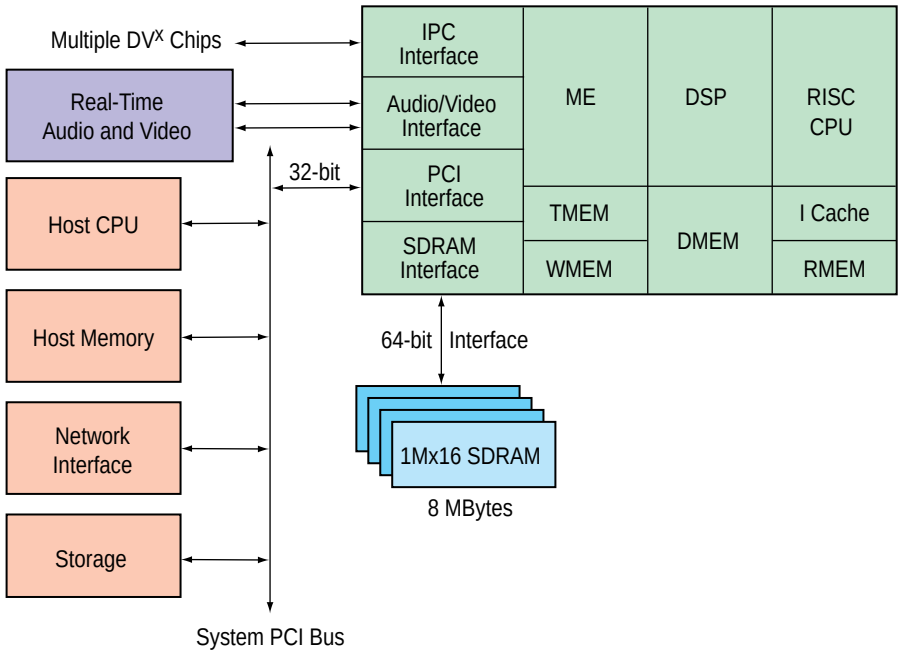
High Degree of Integration. The DV^x architecture enables MPEG-2 solutions that use fewer chips, require less power, and result in smaller circuit boards. This efficiency not only reduces the size of the end product, it improves time-to-market by simplifying the design. And it increases reliability by cutting down on the number of components and providing a cooler operating environment.

Low Memory Requirements. DV^x requires as little as 8 MB of unified memory, for both encoding and decoding. There is no need for additional FIFOs and instruction memory, so design is simplified and system costs are reduced.

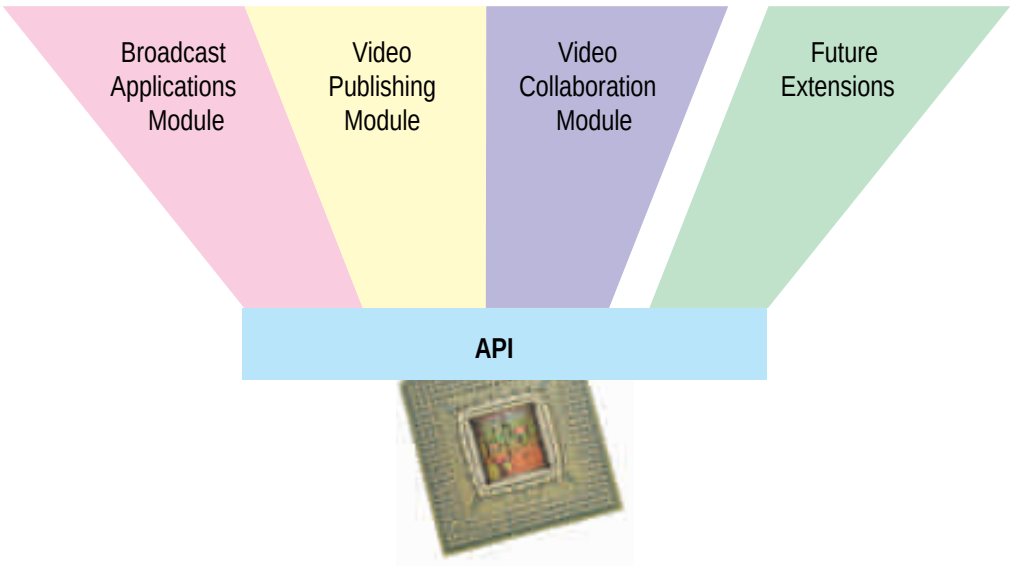
Audio Support. DV^x supports input and output of uncompressed audio data for synchronization with video data.

Programmable Filters. Horizontal and vertical input and output filters, and temporal I/O programmable filters decimate images at the input, helping to produce clear, sharp pictures at the output—at no extra cost.

80 MBytes/Sec Inter-Chip Connection. This high-speed connection lets designers daisy-chain multiple devices to accommodate higher performance applications such as HDTV encoding.



DV^x Platform Architecture Block Diagram



DV^X Unified Application Programming Interface (API)

Unified Application Programming Interface (API). The uniform software design of DV^x means there's no need to develop separate software modules for encoder, decoder, or codec functions.

Superior Video Quality. C-Cube's proprietary PerfectView MPEG-2 compression algorithm ensures the highest picture quality at all bit rates. PerfectView features include:

- Advanced, multilayer motion estimation
- Improved error masking to eliminate common MPEG artifacts
- Inverse telecine for more efficient encoding of film-based material
- Proprietary quality metrics to ensure optimal bit allocation for every picture

Flexible Bit Rate Control. DV^x offers solutions that maximize image quality for a variety of applications:

- Advanced single pass and multipass variable bit rate (VBR) encoding for optimizing Digital Video Disc (DVD) and DVD-RAM applications
- Statistical multiplexing for multichannel broadcast applications
- Constant bit rate (internally controlled or externally signalled) for optimizing fixed rate applications

Variable GOP Structure. Group of Picture (GOP) options include I-frame, IP, IB, IBP, and IBBP, with variable M.

Real-Time Control. On-the-fly control over encoding operation, including real-time adjustment of input resolution and GOP structure.

HDTV Formats. DV^x is the first video compression architecture with the processing power to support all the HDTV formats proposed by the Advanced Television Systems Committee (ATSC).

4:2:2 Encoding. DV^x handles the more advanced 4:2:2 chroma format as well as the 4:2:0 format, providing a single platform for the broad spectrum of professional and prosumer applications.

Multiple-Stream Decoding with Integral Post-Processing. DV^x incorporates technologies, exclusive to C-Cube, that support simultaneous decoding of multiple video streams. In addition, decoding operations are supplemented with an extensive set of post-processing capabilities, including video special effects and on-screen displays.

Low Latency Encode/Decode (Codec). DV^x supports low delay encoding and decoding operations required for video communication applications.

TARGET APPLICATIONS

The flexibility inherent in DV^{x} makes it possible for the architecture to support a wide range of applications through downloadable microcode. These applications include:

- Broadcast over satellite, cable, and Multichannel Multipoint Distributed Service (MMDS) networks
- High-quality studio-to-studio distribution
- Low-delay video communication for electronic news gathering
- Nonlinear video editing
- Compression and disk storage of video content for DVD authoring and video servers
- Video collaboration: Two-way video for distance learning and telemedicine

Electrical Interface Specifications

Video Input/Output Interfaces	CCIR-656 Parallel D1
Audio Input/Output Interfaces	I^2S Compatible, up to 8 channels
Host Interface	PCI Rev 2.1
Test Interface	IEEE 1149.1 (JTAG)
Input Voltage	3.3V (5V I/O tolerance)
System Clock	100 MHz
Package	352 BGA

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